Simulation methodology for Large-Bandwidth Track-and-Hold microwave circuit

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***Abstract*—A step-by-step simulation methodology for large-bandwidth Track-and-hold (T/H) microwave circuit is proposed. A T/H circuit is characterized accurately under the Cadence© environment. With the consideration of a specific windowing function, linearity simulation analysis could be done effectively. Moreover, the use of an input frequency generation function, in accordance with theoretical calculation, allows to treat the entire input bandwidth (BW). A simulated switched emitter follower (SEF) structure in a 0.13-μm SiGe BiCMOS technology with 24 GHz effective bandwidth and a 4 GS/s clock illustrates our methodology.**

I. Introduction

A classical microwave receiver is composed of a low noise amplifier (LNA), a mixer and a Track-and-hold (T/H) circuit in front of the analog-to-digital-converter (ADC) [1]. Usually, frequency mixing requires space and consumes power. Therefore, a T/H circuit with sub-sampling action, could replace positively the mixer and the LNA if the target specifications in terms of noise are compatible. Such circuits present different facets which require different analysis in track/hold mode and in sampling mode. Until now, some articles cover the subject in terms of specific analyses [2],[3]. The aim of this paper, is to propose a step-by-step methodology to cover principal aspects of large bandwidth (BW) T/H circuits and to overcome analysis problem. In addition, the use of a simple windowing function, which allows to process the signal when linearity analysis must be done, is introduced. Moreover, a process able to generate adequate input frequencies in sub-sampling mode is detailed. The purpose analysed architecture is based on the most common used structure the switched emitter follower (SEF) [4],[5] and principal specifications are demonstrated.

In the next section, the considered simulation environment is described. Section III presents the possible simulation scenario, and section IV concludes the paper.

II. Specific environment simulation

For our analysis, we considered the schematic of Fig. 1 under Cadence© design environment. The schematic is based on a differential approach, but it could be used for single-ended structure. For sake of simplicity, we do not consider in our analysis the output buffer and we assume that an ideal quantizer is used. Regarding the microwave clock, we considered a sinusoidal one. The device under test (DUT) is based on the SEF structure of Fig. 2.

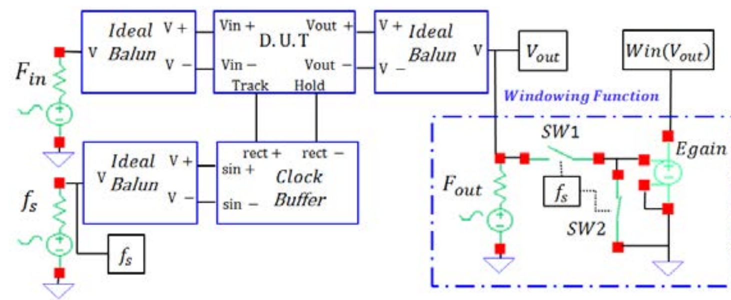

Fig. 1. The used environment for T/H circuit simulation

A. Simulated Switched emitter follower

In track mode, $Q3$, $Q4$, $Q5$ and $Q8$ are ON, thus capacitor C_{Hold} is loaded. In hold mode, $Q7$, $Q6$ are ON, hence added currents in Rl creates drop voltages and $Q3$, $Q4$ are blocked. The added capacitors $C_F \simeq C_{be}$ enhance the isolation against input signal feed-through [6].

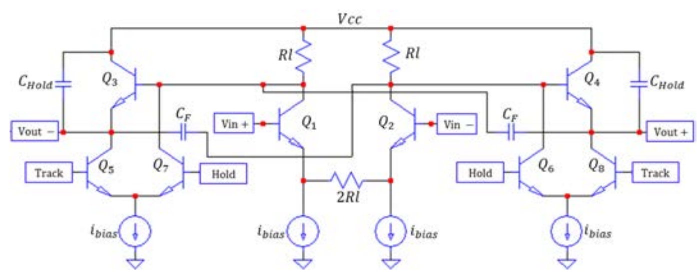

Fig. 2. The simulated large bandwidth T/H structure

B. Rectangular windowing function

In order to simulate this structure periodic steady state (PSS) analysis combined with periodic X frequency (PXF) analysis could be used with the special sampled option. However, the linearity simulation with Quasi Periodic Steady State (QPSS) analysis will be impacted by the zero-hold nature of the DUT [2]. Our solution consists in treating the hold part of the signal with a windowing-rectangular function to approximate a discretized sample as closely as possible. Considering $V_{out}[t]$ the output signal, the equivalent response of windowing function in frequency domain with $0 < \alpha \leq 0.25$ is:

$$W_{in}(\omega) = \int_{-Te\cdot\alpha}^{Te\cdot\alpha} V_{out}[t] \exp^{-j\omega t} dt, \tag{1}$$

$$Egain * W_{in}(f) = Te \cdot Sinc[\alpha 2\pi F_{out} Te]. \tag{2}$$

To be efficient, the chosen value of duty cycle α should be equal to the hold time divided by two or more. With the sampling clock $f_s = 1/Te$, assuming that the input signal is maintained during $Te/2$, $\alpha \leq 0.25$ and $Egain = 1/\alpha$.

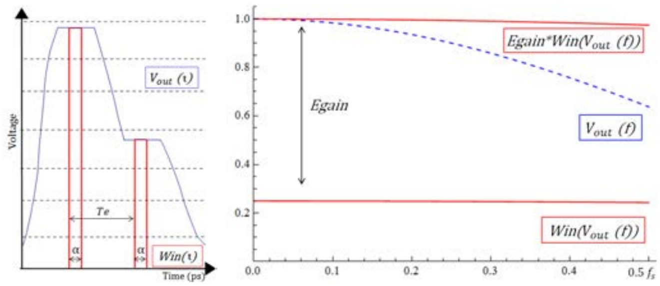

Fig. 3. (a) Illustration of the windowing function on the signal and (b) the equivalent frequency response for $\alpha = 0.25$,we can observe how the linear gain compensate the attenuation

Such function could be done with the implementation of an ideal VerilogA T/H but, because of hidden-state, it will increase simulation time and complexity [7]. In consequence of this limitation we use a couple of complementary switches $SW1/SW2$ piloted by the input clock signal (Fig. 1). The clock synchronization is used for QPSS simulation convergence, therefore it will also be used to control the switches. We combine it with an ideal buffer gain $Egain$ to compensate the linear attenuation coming from the function (2) as shown in Fig. 3. The complementary switches must be closed/opened during the determined windowing time.

C. Input frequency generation function

One of the interesting applications of a large bandwidth T/H is the capability to translate numerous frequencies located in different Nyquist bands into baseband. In order to use QPSS results to calculate total harmonic distortion (THD), it is useful to know the frequencies values created by non-linearity.We assume that major non-linear contributions come from third and second harmonics, therefore (THD) can be express:

$$THD = \frac{\sqrt{P_{H2}^2 + P_{H3}^2}}{P_{Fund}}. \quad (3)$$

Where P_{Hn} is the power of the corresponding harmonic n. The following Fig. 4 shows how to choose correctly the input frequencies (F1,F2..Fn) in order to produce, in baseband, the same fundamental (Fund), the same harmonic 2 (H2) and the same harmonic 3 (H3).

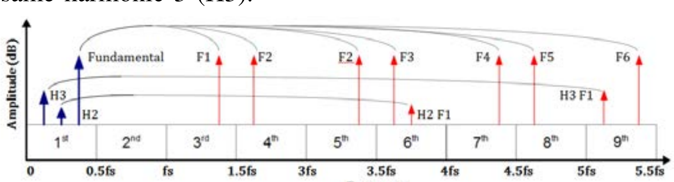

Fig. 4. Input harmonics generation used to analyze the full input spectrum, numbers indicated nyquist bands which is considered under sub-sampling modes

Using right input frequencies it is easier to simulate large BW T/H and generated frequencies can be reuse further to characterize the structure in measurements. In the case that we consider a bandpass signal with a frequency range f_l (lower frequency) to f_u (upper frequency), then we have to respect Nyquist condition sampling frequency $f_s > 2B$ with the band $B = f_u - f_l$. When considering sub-sampling, the band is located at an integer number of bandwidth [8]. Considering the location k of the output frequency $Fout$ in the band B, with $k \in \mathbb{Q}$, the relation can be written :

$$B = \frac{fs}{2}, \; k = \frac{Fout}{B}. \quad (4)$$

If we consider the track input bandwidth (BW) and the clock frequency (f_s) we can calculate the total number of Nyquist Band $N_B \in \mathbb{Q}$ and the corresponding Nyquist band number $n \in \mathbb{N}^*$:

$$N_B = \frac{BW}{fs}, \; 1 < n < N_B \quad (5)$$

The Nyquist location of a sub-sampling frequency depends on its location into the band and can be expressed as:

$$Fin = B(n_{odd} - 1 + k), \; Fin = B(n_{even} - k) \quad (6)$$

Combining the equation (4), with equation (5) and considering equation (6) we found the relation between the output and the input. Equivalent equation can be written in function of two coefficients $a \in \mathbb{N}^*$ and $b \in \mathbb{N}^*$ depending on the Nyquist band location n:

$$Fin = \frac{fs}{2}(a + \frac{2}{fs} b \cdot Fout). \quad (7)$$

Depending on a and b the input frequency is defined by the following modulo ($MOD(x, \mathbb{N})$) operation for a fixed $Fout$:

$$a = n - MOD(n, 2) \; , \; b = 2 * MOD(n, 2)\text{-}1. \quad (8)$$

Using the previous equation (7), it is straightforward to calculate harmonic 2 and harmonic 3 values in order to calculate THD (3):

$$n_{H2} = floor(\frac{2Fin}{0.5fs}), \; n_{H3} = floor(\frac{3Fin}{0.5fs}), \quad (9)$$

$$Fout_{H2} = \frac{1}{b}(2Fin\text{-}\frac{fs}{2}a), \; Fout_{H3} = \frac{1}{b}(3Fin\text{-}\frac{fs}{2}a). \quad (10)$$

For example, with $f_s = 4$ GHz ,$BW = 24$ GHz and $Fout = 1.2$ GHz we can calculate corresponding input frequencies witch fall in the 11th Nyquist band. With B=2 GHz, $k = \frac{Fout}{fs} = \frac{3}{5}$, $N_B = 12$. For $n_{odd} =$ 11 we calculate :

$$Fin_{11} = B(n_{odd} - k) = 2 \cdot 10^9 \cdot (\frac{52}{5}) = 20.8 \text{ GHz}. \quad (11)$$

Using equation (10) and equation (7) in an Ocean© script, combined with QPSS analysis , the input frequencies can be generated depending on the desired output frequency as showed in Fig. 4. After implementation of the described function we can follow up with the different analysis.

III. Dedicated simulations for T/H circuits

Track and hold circuits could be simulated in track mode or in sampling mode. Depending on performance the designer want to simulate, the dedicated environment in Table I allows to treat all the simulation scenarios. Considering a microwave circuit, scattering parameters (SP) small signal analysis is commonly used. The following table resumes the principal simulations executed by order and detailed in this paper.

TABLE I
Simulations done with SpectreRF© executed by order

Simulation Analysis	Track mode	Step	Sampling mode	Step
Bandwidth	SP	1^{st}	PSS-PXF	2^{nd}
Noise Figure	SP-Noise	3^{rd}	PSS-Pnoise	4^{th}
THD/P-1dB	PSS	5^{th}	QPSS	6^{th}

A. Bandwidth

One of the main interest of our circuit is to obtain a high input bandwidth (BW) therefore we start by the $\mathbf{1^{st}}$ analysis to obtain the input bandwidth. In Fig. 5 the scattering parameter ($S_{[2,1]}$) in function of F_{in} is plotted showing a value of 28 GHz at -3 dB which corresponds to the effective BW. After the consideration of the input bandwidth in track mode, we now concentrate on the sampling mode.

The $\mathbf{2^{nd}}$ analysis is done in frequency-domain through a PSS analysis with $f_s = 4$ GHz. This one allows to compute the impulse response of the system. Secondly, PXF analysis is chosen with sampling option. This analysis will compute all the transfer functions of the inputs with regard to one selected output. Considering the right sample, we can obtain conversion loss of the T/H and compare track bandwidth to sampling-bandwidth impacted by conversion loss.

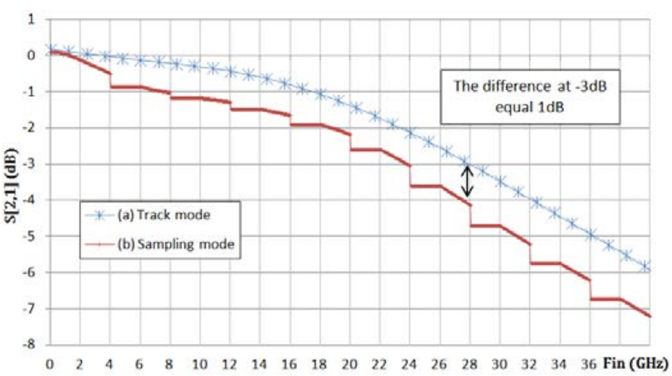

Fig. 5. Obtained scattering parameter S(2,1) in respect to input frequency in (a) track mode and (b) in sampling mode sliced by f_s

The comparison of both curves in Fig. 5, shows that the input track gain at -3 dB decreases by 1 dB with conversion losses. Therefore, the final effective input BW is equal to 24 GHz. In parallel, it is important to size the output isolation during the hold-mode to quantify the feed-through:

$$Isolation_{\text{dB}} = S_{[2,1]\text{dB}|Hold}\text{-}S_{[2,1]\text{dB}|Track}. \quad (12)$$

We shall pay a particular attention to the considered direct bias current (dc) in this mode. When a load is applied at the output of the circuit, a non-realistic isolation could-be obtained as illustrated in Fig. 6 (b). The problem comes from the initial conditions (ic). Because of a leaking current in the output load, the considerate ic is wrong and corresponding dc will never exist in sampled mode. In order to overcome this problem we may force the capacitor voltage to a value equivalent to a possible held value Fig. 6 curve (a).

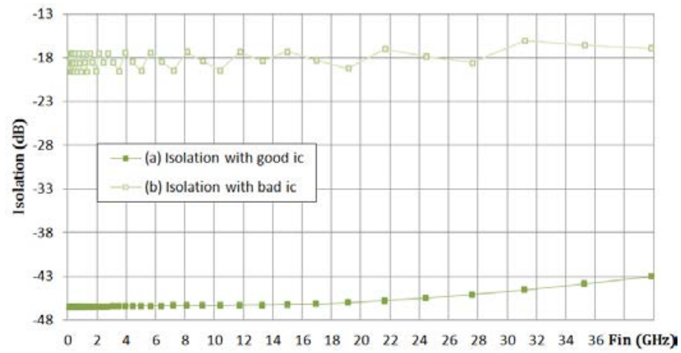

Fig. 6. Obtained output isolation (12) from the input in Hold mode (a) with good initial condition (b) with bad initial condition

B. Noise Figure

Commonly, thermal noise in sampled circuits is the main noise source [3]. This noise is linked to an equivalent resistive element in the circuit which is uniformly distributed. Its spectral density is equal $4kTR$, were k is the Boltzman constant, T is the temperature in kelvin and R is the equivalent resistor. We sample the stationary input noise every $1/f_s$, therefore the resulting noise is cyclostationary [9] and aliased in baseband. Theoretical calculation of an aliasing noise P_{als} with a first order transfert function for the input bandwidth (BW) under a single-side-band consideration (SSB) [2], has to be taken:

$$P_{als|dB} = 10 \cdot Log(\frac{\pi}{2} BW \cdot \frac{1}{0.5 f_s}). \quad (13)$$

From the previous calculation the noise factor NF_{Sample} in sampling mode can be approximate by:

$$NF_{Sample} = P_{in|dBm}\text{-}P_{kT|dBm}\text{-}P_{BW|dB}\text{-}P_{als}\text{-}SNR_{out}. \quad (14)$$

With P_{in} is the input power of the signal, P_{kT} is a noisy 50 Ω resistor, P_{BW} is the equivalent noise input bandwidth and SNR_{out} is the signal to noise ratio at the output. In track mode the noise factor NF_{Track} is expressed by:

$$NF_{Track} = SNR_{in}\text{-}SNR_{out}, \; SNR_{in} = P_{in}\text{-}P_{kT}\text{-}P_{BW}. \quad (15)$$

In accordance with theoretical result, noise analysis simulation can be done. To perform a good check of results, we start by evaluating the noise in the track mode.

The $\mathbf{3^{rd}}$ step is carried out using noise source option in SP parameter analysis and plotted in Fig. 7 . The obtained results show an average value of $NF_{Track} \simeq 13$ dB.

The $\mathbf{4^{th}}$ simulation step concerns the cyclostationary noise, it requires a specific analysis through a PSS, followed by a specific Periodic noise (P-noise) in sampling mode. In this paper all the simulations are done using fs=4 GHz and a power input signal of P_{in}=-6 dBm. The last result shows a average value of $NF_{Sample} \simeq 28$ dB.

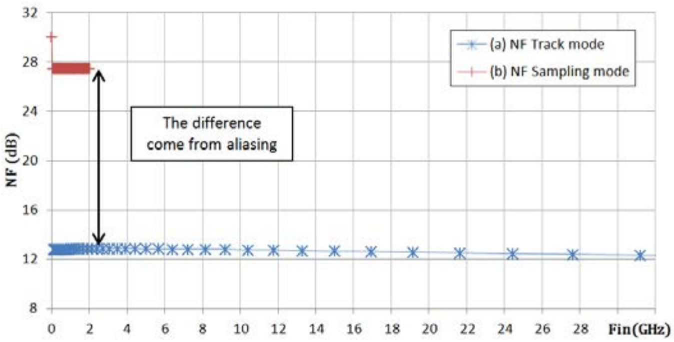

Fig. 7. Obtained Noise figure in (a) track mode and (b) sampling mode, we can observe how the noise increase by aliasing effect

The observed difference in Fig. 7 results from the contribution of aliasing noise into baseband. The comparison of the theoretical calculation $P_{als|cal} \simeq 14$ dB (13) with the plotted simulated results $P_{als|sim} \simeq 13$ dB Fig. 7, shows a small difference of 1dB. This difference comes from the consideration of an approximate value for the input bandwidth BW=24 GHz in the $P_{als|cal}$ calculation. After achieving verification of the obtained $NF_{sampling}$ value we can calculate the SNR_{out}. Under a SSB consideration the SNR_{out} value equal to 47 dB. Once the final SNR_{out} is evaluated, the linearity specification could be analyzed.

C. Linearity

According to [10], we start by calculating the compression point at 1dB (P_{1dB}) from specifications. Here, for example we calculate a minimal $P_{1dB} \simeq 2$ dBm for one tone excitation. Using the compression function in PSS analysis, we obtain the following curve in track mode with one tone excitation :

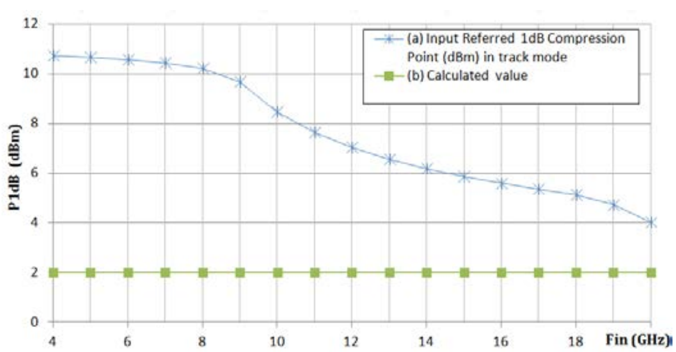

Fig. 8. Obtained $P1$ dB from extrapolation at -20 dBm input power P_{in} in (a) track mode and (b) calculated value

The obtained simulation results indicates that our targeted P_{1dB} is not reached. Based on this calculation we continue with the $\mathbf{5^{th}}$ analysis in order to obtain THD (3) in track mode Fig. 9. We are now interested in the linearity of the T/H in sampling mode, hence we consider the $\mathbf{6^{th}}$ analysis. By using windowing function, it is possible to directly obtain the magnitude of the different harmonics. Using the generation function described previously to simulate the THD, we obtain the following result:

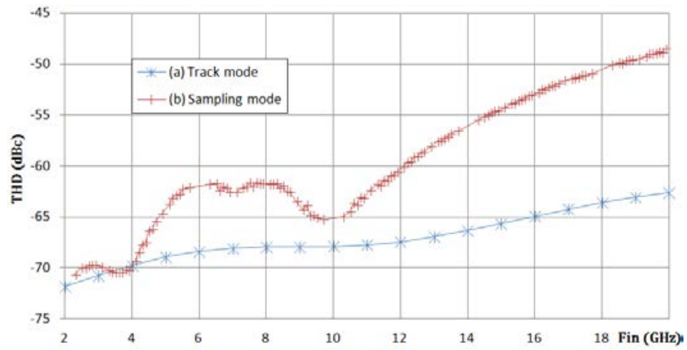

Fig. 9. Obtained THD in (a) track mode and (b) sampling mode

Considering the ideal current sources used and the Harmonic 2 reduction by differential operation, the worst average $THD_{sampling} \simeq$ -48 dB. In track mode the worst average $THD_{Track} \simeq$ -63 dB is significantly lower. The difference between the two curves comes from the non-linearity created by mixing products between the clock and input signal.

IV. Conclusion

We have detailed how to simulate a large bandwidth T/H circuit through a step-by-step methodology. Based on analytical calculation we demonstrated the validity of the results obtained by simulation. In addition, the use of a specific generation frequency function combined with a windowing function demonstrates how to analyze the linearity of the structure over a large input spectrum. Regarding simulated results, we concluded that high performance T/H microwave circuit can be efficiently analyzed under the Cadence© environment with our methodology.

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